AMENDMENT TO CLAIMS

The listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

Claims 1-36 (cancelled)

Claim 37 (Currently Amended) A method, comprising:

assigning a group of instructions selected from a plurality of groups of instructions partitioned from a program, to a subset of interconnected computation nodes preselected from a plurality of interconnected computation nodes, the instructions having associated operands;

loading a subset of instructions of the assigned group of instructions into a frame of buffers comprising stores disposed on the subset of interconnected preselected computation nodes having been assigned the group of instructions, prior to the associate operands of the subset of instructions are available ~~having all necessary associated operands for execution~~;

receiving associated operands of the subset of instructions by the preselected computation nodes, including a first of the preselected computation nodes directly receiving a first associated operand of a first instruction loaded into the first preselected computation node, from a second of the preselected computation nodes, wherein the first computation node has an input port capable of being coupled to the second computation node to enable the directly receiving of the first associated operand; and

executing the subset of instructions as each one of the instructions in the subset of instructions loaded into the frame of buffers receives associated operands for execution.

Claim 38 (Currently amended) The method of claim 37, ~~wherein at least one computation node included in the plurality of interconnected preselected computation nodes has at least one input port capable of being coupled to at least one preselected first other computation node included in the plurality of interconnected preselected computation nodes, the input port to receive input data,~~ further comprising storing the first associated operand in a first store of the first computation node, wherein the first store is coupled to the ~~at least one~~ input port ~~to store the input data~~, storing the first instruction in a second store of the first computation node, wherein the

second store is coupled to an instruction sequencer, ~~the second store to receive and store the at least one instruction~~, matching the first associated operand with the first instruction by an instruction wakeup unit ~~to match the input data to the at least one instruction~~, ~~at least one~~ executing the first instruction by an execution unit of the first computation node ~~to execute the at least one instruction~~ using at least the ~~input data~~first operand to produce output data, and ~~at least one~~routing the output data to an output port of the first computation node, wherein the output port is capable of being coupled to ~~at least one second other~~a third of the preselected computation node~~s included in the plurality of interconnected preselected computation nodes, and a router~~ to directly provide the output data ~~from the at least one output port to the at least one preselected second other~~ to the third preselected computation node.

Claim 39 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a basic block.

Claim 40 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a hyperblock.

Claim 41 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is a superblock.

Claim 42 (Previously Presented) The method of claim 37, wherein at least one of the plurality of groups of instructions is an instruction trace constructed by a hardware trace construction unit at run time.

Claim 43 (Previously presented) The method of claim 37, wherein loading the subset of instructions into a frame of buffers comprising stores disposed on the subset of interconnected preselected computation nodes includes:

sending at least two instructions selected from the group of instructions from an instruction sequencer to a selected computation node included in the subset of interconnected

preselected computation nodes for storage in a store of the selected computation node, prior to the at least two instructions having all necessary associated operands for execution.

Claim 44 (Previously presented) The method of claim 37, wherein executing the subset of instructions loaded into the frame of buffers as each one of the instructions in the subset of instructions receives associated operands for execution includes:

matching at least one instruction selected from the subset of instructions with at least one operand received from an other computation node included in the subset of interconnected preselected computation nodes.

Claim 45 (Cancelled)

Claim 46 (Previously presented) The method of claim 37, further comprising concurrently assigning another group of instructions selected from the plurality of groups of instructions to another or the same subset of interconnected preselected computation nodes for concurrent execution using one or more other frames of buffers comprising stores disposed on the another or same subset of interconnected preselected computation nodes, wherein the two groups of instructions are capable of concurrent execution.

Claim 47 (Currently amended) An article comprising a machine-accessible medium having machine executable instructions stored therein, if executed, enable a machine to:

assign a subset of a group of instructions selected from a plurality of groups of instructions partitioned from a program, to a subset of interconnected computation nodes of the machine, the instructions having associated operands; and

load thea subset of a group of instructions ~~selected from a plurality of groups of instructions partitioned from a program,~~ into a frame of buffers comprising stores disposed on the a subset of interconnected preselected computation nodes ~~preselelcted from a plurality of interconnected preselelcted computation nodes, and assigned to execute the subset of instructions~~, wherein the subset of the group of instructions is loaded into the frame of buffers prior to the

associated operands of the subset of the group of instructions are available ~~having all necessary associated operands for execution~~;

wherein the loaded instructions are executed as each one of the instructions receives associated operands for execution,

wherein receive associated operands includes at least a first of the subset of computation nodes directly receiving a first associated operand of a first instruction from a second of the subset of interconnected computation nodes coupled to the first computation node.

Claim 48 (Previously presented) The article of claim 47, wherein the machine executable instructions, if executed, further enable the machine to partition the program into the plurality of groups of instructions during compilation of the program.

Claim 49 (Previously presented) The article of claim 47, wherein the machine executable instructions, if executed, further enable the machine to partition the program into the plurality of groups of instructions is performed during run-time.

Claim 50 (Previously presented) The article of claim 47, wherein the machine-accessible medium further includes instructions, if executed, enable the machine to statically assign each of the plurality of groups of instructions to a subset of interconnected preselected computation nodes preselected from a plurality of interconnected computation nodes for execution.

Claim 51 (Cancelled)

Claim 52 (Currently amended) The article of claim 47, wherein the machine-accessible medium further includes instructions, if executed, enable the machine to generate a wakeup token to reserve an output data channel of the second computation node to directly route the first associated operand from the second computation node to the first computation node~~connect selected computation nodes included in the subset of preselected interconnected computation nodes~~.

Claim 53 (Previously presented) The article of claim 47, wherein the machine-accessible medium further includes instructions , if executed, enable the machine to repeat said loading until the entire group of instructions are executed, and to detect execution termination of the group of instructions including an output having architecturally visible data; and committing the architecturally visible data to a register file.

Claim 54 (Previously presented) The article of claim 47, wherein the machine-accessible medium further includes instructions , if executed, enable the machine to repeat said loading until the entire group of instructions are executed, and to detect execution termination of the group of instructions including an output having architecturally visible data; and committing the architecturally visible data to a memory.

Claim 55 (Previously presented) The article of claim 47, wherein the machine-accessible medium further includes instructions, if executed, enable the machine to route an output datum arising from executing one of the subset of instructions to a consumer node included in the plurality of interconnected preselected computation nodes, wherein the address of the consumer node is included in a token associated with at least one instruction included in the subset of instructions.

Claim 56 (Currently amended) The method of claim 37 further comprising repeating said loading and executing until the entire group of instructions have been executed.

Claim 57 (Currently amended) An apparatus, comprising:

a plurality of interconnected computation nodes; and

storage medium coupled to the processor and ~~having~~ configured to have first instructions stored therein to be executed by the processor, wherein the first instructions are configured to:

assign a group of second instructions selected from a plurality of groups of second instructions partitioned from a program to a preselected subset of the plurality of interconnected computation nodes, the second instructions having associated operands; and

causing a subset of the second instructions of the assigned group of second instructions to be loaded into a frame of buffers comprising stores disposed on the subset of interconnected computation nodes having been assigned the group of second instructions, prior to the associated operands of the subset of the second instruction are available~~having all necessary associated operands for execution~~, wherein at least a first of the associated operands of a first of the second instructions loaded into a first of the preselected computation nodes is directly received from a second of the preselected computation nodes, wherein the subset of second instructions are executed as each one of the instructions in the subset of second instructions loaded into the frame of buffers receives associated operands for execution.

Claim 58 (Previously presented) The apparatus of claim 57, wherein at least one of the plurality of groups of second instructions is a selected of one a basic block, a hyperblock or a superblock.

Claim 59 (Cancelled)

Claim 60 (Currently amended) A system, comprising:

a plurality of interconnected computing nodes configured to be pre-selectable to cooperatively execute a subset of a group of instructions, wherein the group is one of a plurality groups of instructions partitioned from a program and the instructions have associated operands;

wherein individual of the interconnected computing nodes includes:

computing resource including an execution unit configured to execute instructions; and

interconnect resource coupled to the computing resource to enable the computing node to cooperate with the other interconnected computation nodes to execute the group of instructions by successively executing ~~subgroups~~ subsets of the group of instructions;

wherein the interconnect resource includes:

at least one input port capable of ~~being coupled~~directly coupling the computing resource to at least a first other preselected computation node included

in the plurality of interconnected preselected computation nodes, and the input port is configured to receive input data,

a first store coupled to the at least one input port, and configured to store the input data,

a second store coupled to the execution unit, ~~the second store~~and configured to receive and store at least one instruction of a subgroup, the second store being a part of a frame of buffers spanning the plurality of interconnected preselected computation nodes to store a subgroup of instructions loaded into the frame of buffers prior to the associated operands of the the subgroup of instructions are available ~~having all necessary associated operands for execution~~,

an instruction wakeup unit to match the input data to the at least one stored instruction,

~~at least one~~an output port coupled to the execution unit and capable of ~~being coupled~~directly coupling the computing resource to ~~at least one~~a second other preselected computation node included in the plurality of interconnected preselected computation nodes, and

a router coupled to the execution unit, and configured to direct an output data of the execution unit ~~from the at least one~~to the output port for direct provision to the ~~at least one preselected~~ second other computation node.